

### **39 $\mu$ A Micropower Single and Dual Precision Rail-to-Rail Input-Output (RRIO) Low Input Bias Current Op Amps**

The ISL28156 and ISL28256 are micropower precision operational amplifiers optimized for single supply operation at 5V and can operated down to 2.4V.

These devices feature an Input Range Enhancement Circuit (IREC) which enables them to maintain CMRR performance for input voltages greater than the positive supply. The input signal is capable of swinging 0.5V above a 5.0V supply (0.25 for a 2.5V supply) and to within 10mV from ground. The output operation is rail-to-rail.

The 1/f corner of the voltage noise spectrum is at 1kHz. This results in low frequency noise performance which can only be found on devices with an order of magnitude higher supply current.

ISL28156 and ISL28256 can be operated from one lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail. The output swings to both rails.

#### **Ordering Information**

<b>PART NUMBER (Note)</b>	<b>PART MARKING</b>	<b>TAPE AND REEL</b>	<b>PACKAGE (Pb-Free)</b>	<b>PKG. DWG. #</b>
ISL28156FHZ-T7	GABV	7" (3k pcs)	6 Ld SOT-23	MDP0038
ISL28156FBZ	28156FBZ	97/Tube	8 Ld SOIC	MDP0027
ISL28156FBZ-T7	28156FBZ	7" (1k pcs)	8 Ld SOIC	MDP0027
<i>Coming Soon</i> ISL28256FAZ-T7		7" (1k pcs)	8 Ld SOIC	MDP0027
<i>Coming Soon</i> ISL28256FAZ-T7		7"	8 Ld MSOP	MDP0043

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

#### **Features**

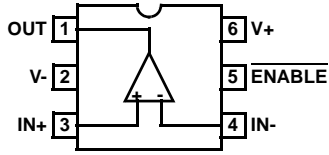
- 39 $\mu$ A typical supply current
- 5nA max input bias current
- 250kHz gain bandwidth product ( $A_V = 1$ )
- 2.4V to 5.5V single supply voltage range
- Rail-to-rail input and output
- Enable pin (ISL28156 only)
- Pb-free plus anneal available (RoHS compliant)

#### **Applications**

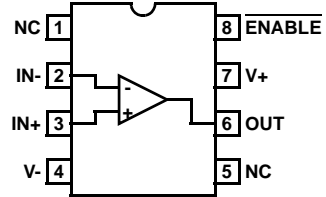
- Battery- or solar-powered systems
- 4mA to 20mA current loops
- Handheld consumer products
- Medical devices
- Sensor amplifiers
- ADC buffers
- DAC output amplifiers

Pinouts

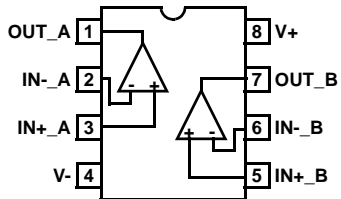
ISL28156  
(6 LD SOT-23)  
TOP VIEW



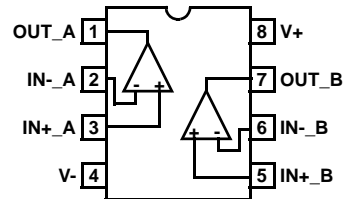
ISL28156  
(8 LD SOIC)  
TOP VIEW



ISL28256  
(8 LD SOIC)  
TOP VIEW



ISL28256  
(8 LD MSOP) *Coming Soon*  
TOP VIEW



**Absolute Maximum Ratings** ( $T_A = +25^\circ\text{C}$ )

Supply Voltage	5.5V
Supply Turn On Voltage Slew Rate	1V/ $\mu\text{s}$
Differential Input Current	5mA
Differential Input Voltage	0.5V
Input Voltage	V- - 0.5V to V+ + 0.5V
ESD tolerance, Human Body Model	.3kV
ESD tolerance, Machine Model	.300V

**Thermal Information**

Thermal Resistance	$\theta_{JA}$ ( $^\circ\text{C}/\text{W}$ )
6 Ld SOT-23 Package	230
6 Ld SO Package	110
8 Ld MSOP Package	115
Output Short-Circuit Duration	Indefinite
Ambient Operating Temperature Range	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Storage Temperature Range	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Operating Junction Temperature	+125 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**Electrical Specifications**

$V_+ = 5\text{V}$ ,  $V_- = 0\text{V}$ ,  $V_{CM} = 2.5\text{V}$ ,  $T_A = +25^\circ\text{C}$  unless otherwise specified.  
 Boldface limits apply over the operating temperature range, -40 $^\circ\text{C}$  to +125 $^\circ\text{C}$ , temperature data guaranteed by characterization

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OS</sub>	Input Offset Voltage	8 Ld SO	-120 <b>-200</b>	-7	120 <b>250</b>	$\mu\text{V}$
		6 Ld SOT-23	-400 <b>-450</b>	-7	400 <b>450</b>	$\mu\text{V}$
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Input Offset Drive vs Temperature			1.5		$\mu\text{V}/^\circ\text{C}$
I <sub>OS</sub>	Input Offset Current		-1.5 <b>-5</b>	0.34	1.2 <b>2.5</b>	nA
I <sub>B</sub>	Input Bias Current		-2 <b>-3.5</b>	1.14	5 <b>5</b>	nA
E <sub>N</sub>	Input Noise Voltage Density	F <sub>O</sub> = 1kHz		46		nV/ $\sqrt{\text{Hz}}$
I <sub>N</sub>	Input Noise Current Density	F <sub>O</sub> = 1kHz		0.14		pA/ $\sqrt{\text{Hz}}$
CMIR	Input Common-Mode Voltage Range		0		5	V
CMRR	Common-Mode Rejection Ratio	V <sub>CM</sub> = 0V to 5V	80 <b>75</b>	110		dB
PSRR	Power Supply Rejection Ratio	V <sub>S</sub> = 2.4V to 5V	90 <b>75</b>	104		dB
A <sub>VOL</sub>	Large Signal Voltage Gain	V <sub>O</sub> = 0.5V to 4.5V, R <sub>L</sub> = 100k $\Omega$	200 <b>175</b>	412		V/mV
		V <sub>O</sub> = 0.5V to 4.5V, R <sub>L</sub> = 1k $\Omega$	35 <b>30</b>	70		V/mV
V <sub>OUT</sub>	Maximum Output Voltage Swing	Output low, R <sub>L</sub> = 100k $\Omega$		3	6 <b>8</b>	mV
		Output low, R <sub>L</sub> = 1k $\Omega$		130	150 <b>200</b>	mV
		Output high, R <sub>L</sub> = 100k $\Omega$	4.992 <b>4.99</b>	4.985		V
		Output high, R <sub>L</sub> = 1k $\Omega$	4.85 <b>4.8</b>	4.88		V
SR	Slew Rate			0.05		V/ $\mu\text{s}$
GBW	Gain Bandwidth Product	A <sub>V</sub> = 1		250		kHz
I <sub>S,ON</sub>	Supply Current, Enabled		29 <b>18</b>	39	47 <b>56</b>	$\mu\text{A}$
I <sub>S,OFF</sub>	Supply Current, Disabled			10	14 <b>16</b>	$\mu\text{A}$

**Electrical Specifications**  $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, T_A = +25^\circ C$  unless otherwise specified.  
 Boldface limits apply over the operating temperature range,  $-40^\circ C$  to  $+125^\circ C$ , temperature data guaranteed by characterization **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{O+}$	Short-Circuit Output Current	$R_L = 10\Omega$	28 <b>23</b>	31		mA
$I_{O-}$	Short-Circuit Output Current	$R_L = 10\Omega$	24 <b>18</b>	26		mA
$V_{SUPPLY}$	Supply Operating Range	Guaranteed by PSRR test	2.4		5	V
$V_{ENH}$	Enable Pin High Level		<b>2</b>			V
$V_{ENL}$	Enable Pin Low Level				<b>0.8</b>	V
$I_{ENH}$	Enable Pin Input Current	$V_{EN} = 5V$	0.7	1	1.2 <b>1.2</b>	$\mu A$
$I_{ENL}$	Enable Pin Input Current	$V_{EN} = 0V$	10	16	25 <b>30</b>	nA
$t_{EN}$	Enable to output on-state delay time (ISL28156)	$V_{out} = 1V$ (enable state); $\overline{V_{EN}} =$ High to Low		10.8		$\mu s$
$t_{\overline{EN}}$	Enable to output off-state delay time (ISL28156)	$V_{out} = 0V$ (disabled state) $\overline{V_{EN}} =$ Low to High		0.1		$\mu s$

**Typical Performance Curves**

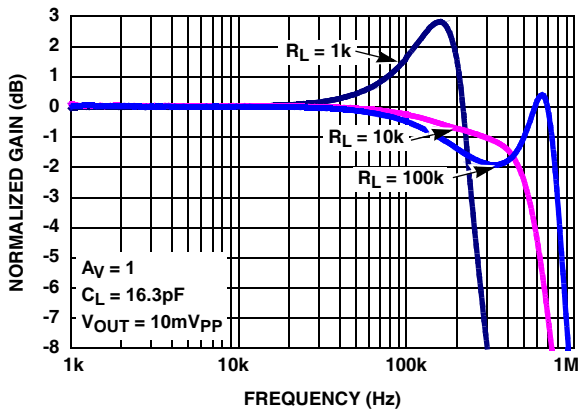


FIGURE 1. GAIN vs FREQUENCY vs  $R_L$

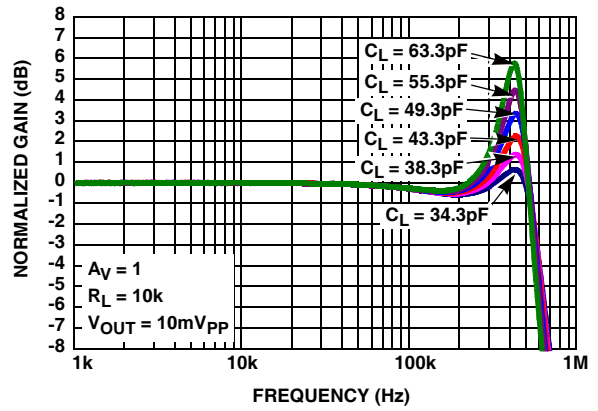


FIGURE 2. GAIN vs FREQUENCY vs  $C_L$

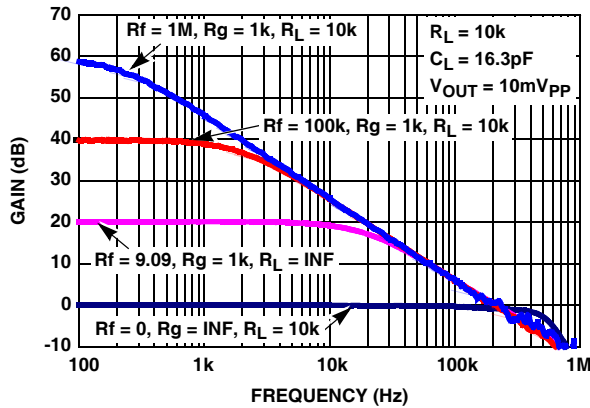


FIGURE 3. CLOSED LOOP GAIN vs FREQUENCY

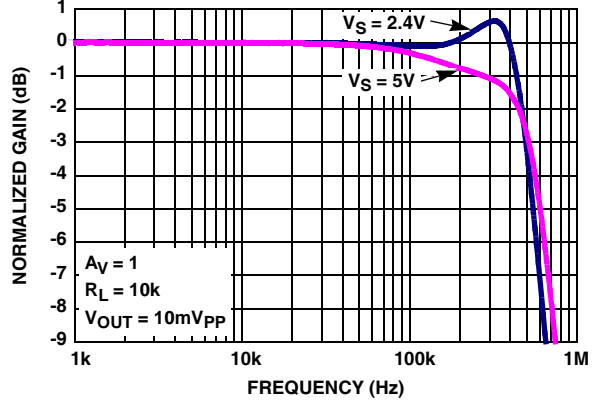


FIGURE 4. GAIN vs FREQUENCY vs  $V_S$

Typical Performance Curves (Continued)

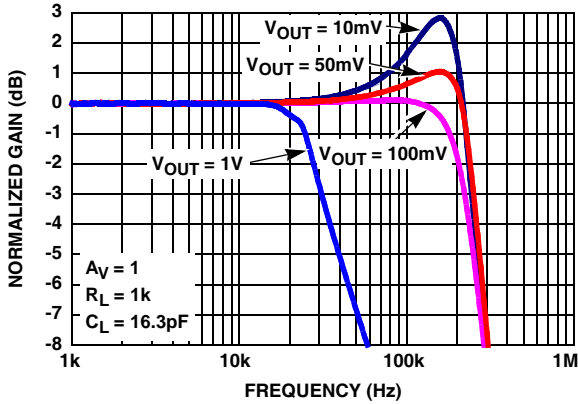


FIGURE 5. GAIN vs FREQUENCY vs  $V_{OUT}$

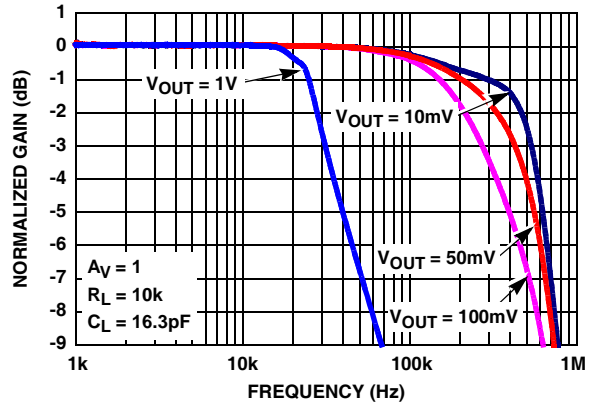


FIGURE 6. GAIN vs FREQUENCY vs  $V_{OUT}$

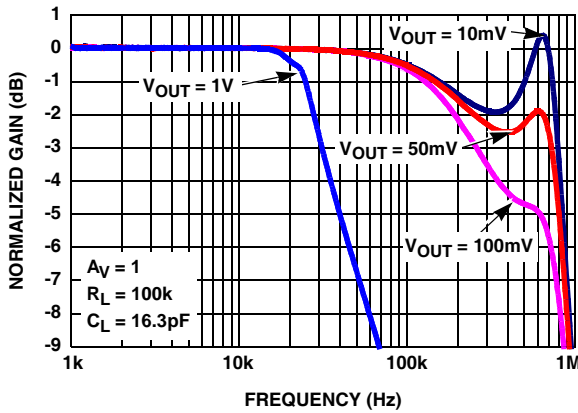


FIGURE 7. GAIN vs FREQUENCY vs  $V_{OUT}$

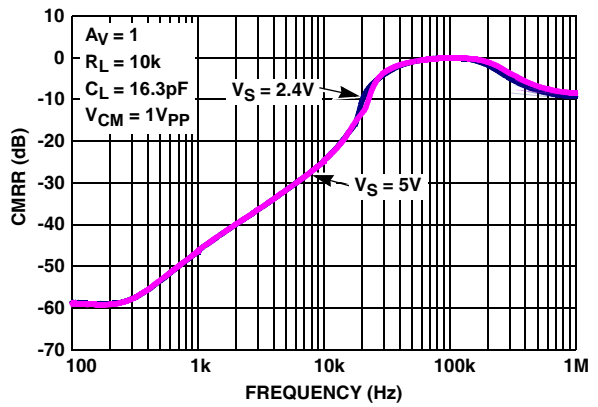


FIGURE 8. CMRR vs FREQUENCY

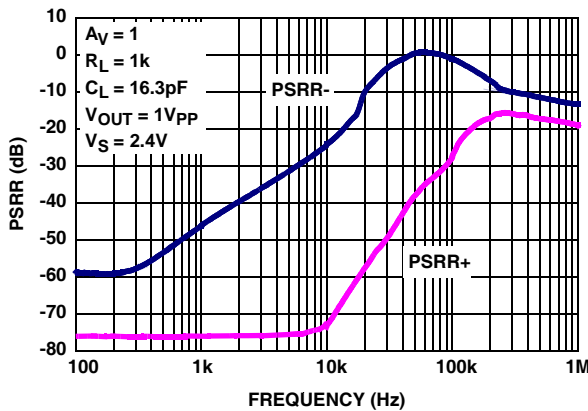


FIGURE 9. PSRR vs FREQUENCY;  $V_S = 2.4V$

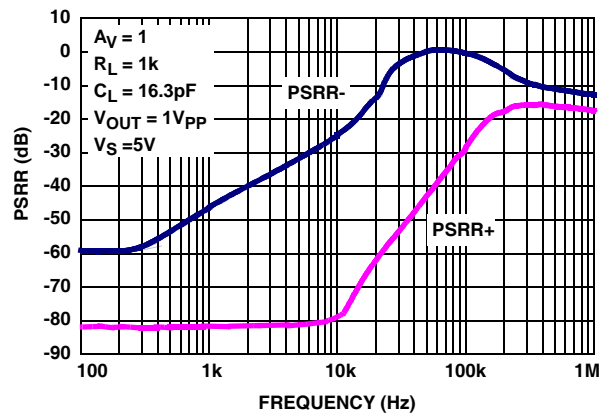


FIGURE 10. PSRR vs FREQUENCY;  $V_S = 5V$

Typical Performance Curves (Continued)

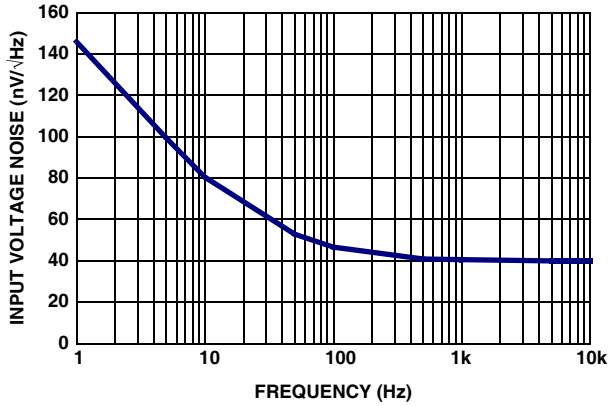


FIGURE 11. INPUT VOLTAGE NOISE vs FREQUENCY

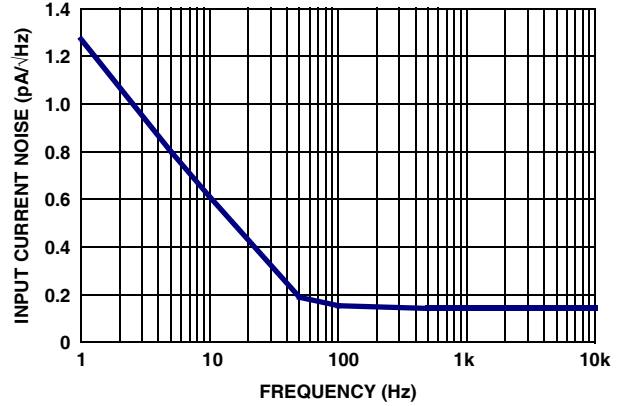


FIGURE 12. INPUT CURRENT NOISE vs FREQUENCY

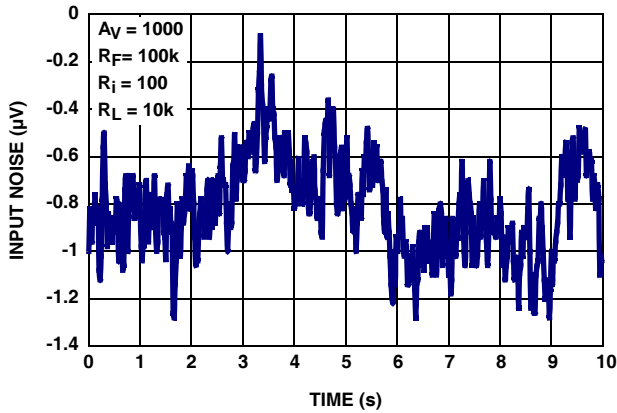


FIGURE 13. 1 TO 10Hz INPUT NOISE

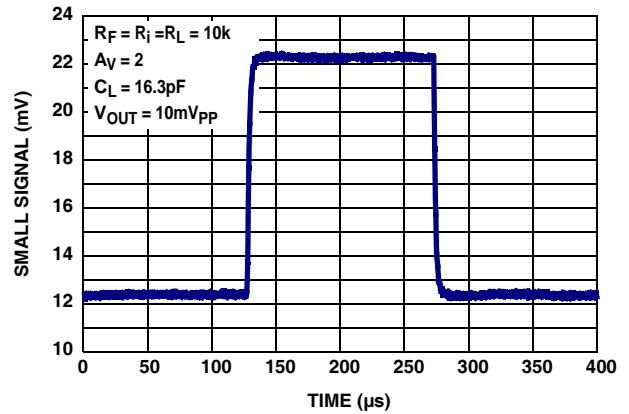


FIGURE 14. SMALL SIGNAL STEP RESPONSE

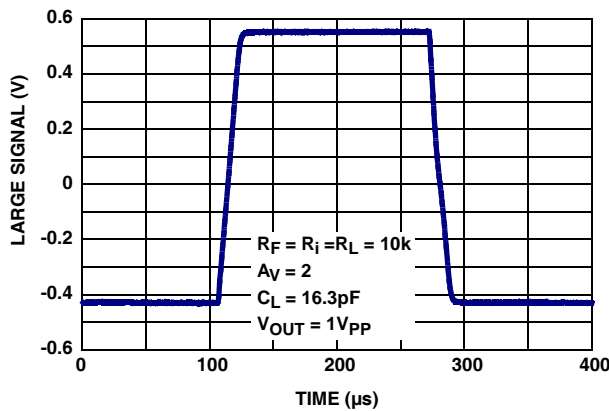


FIGURE 15. LARGE SIGNAL STEP RESPONSE

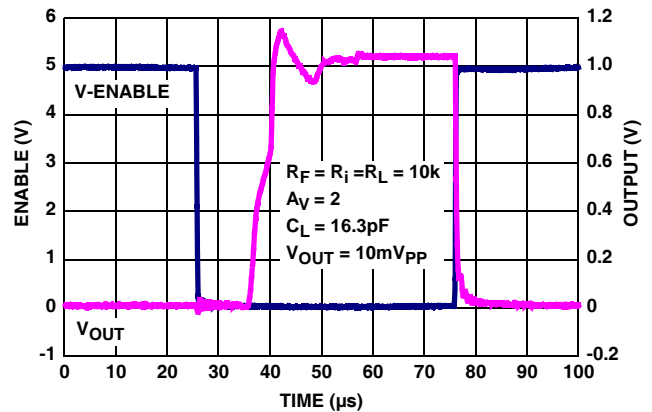


FIGURE 16. ENABLE TO OUTPUT DELAY

Typical Performance Curves (Continued)

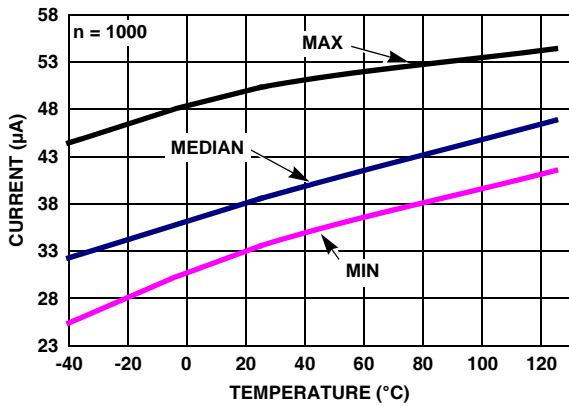


FIGURE 17. SUPPLY CURRENT ENABLED vs TEMPERATURE  $V_S = \pm 2.5V$

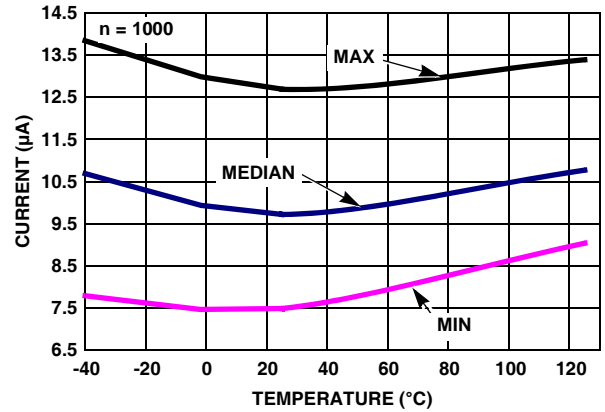


FIGURE 18. SUPPLY CURRENT DISABLED vs TEMPERATURE  $V_S = \pm 2.5V$

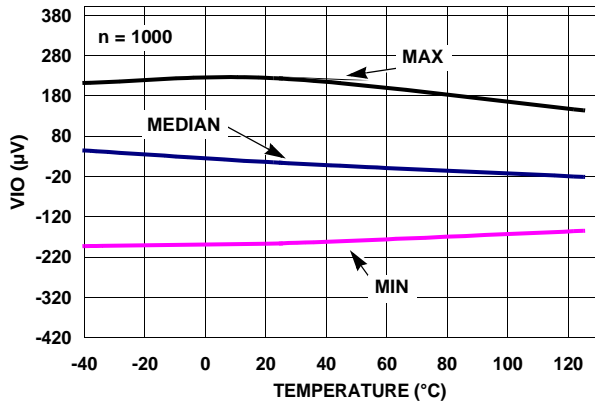


FIGURE 19. VIO SO8 PACKAGE vs TEMPERATURE  $V_S = \pm 2.5V$

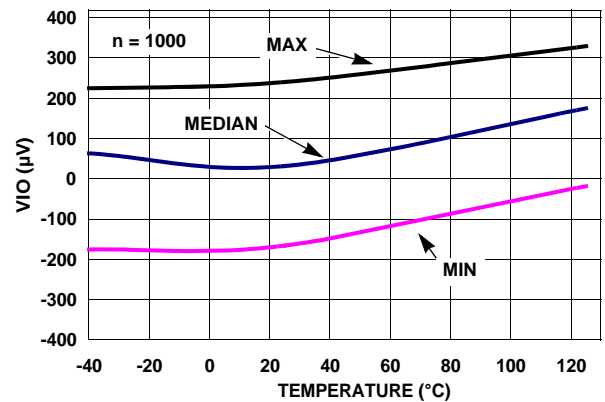


FIGURE 20. VIO SO8 PACKAGE vs TEMPERATURE  $V_S = \pm 1.2V$

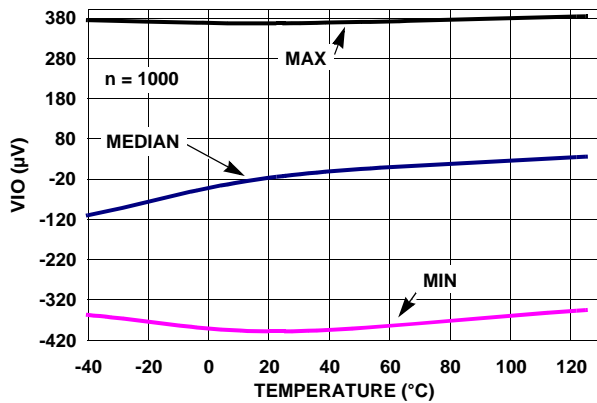


FIGURE 21. VIO SOT-23 PACKAGE vs TEMPERATURE  $V_S = \pm 2.5V$

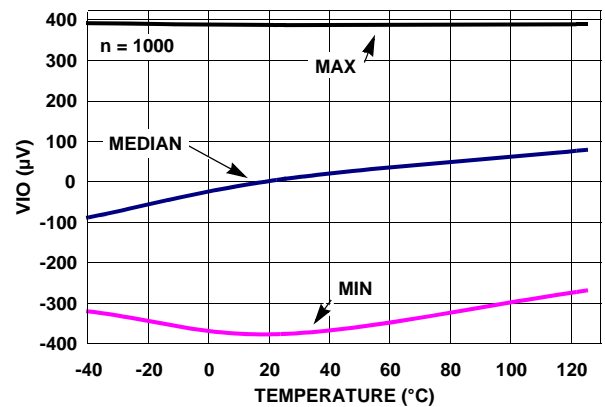


FIGURE 22. VIO SOT-23 PACKAGE vs TEMPERATURE  $V_S = \pm 1.2V$

Typical Performance Curves (Continued)

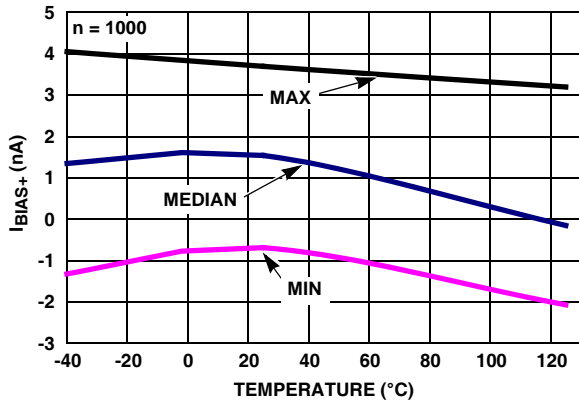


FIGURE 23.  $I_{BIAS+}$  vs TEMPERATURE  $V_S = \pm 2.5V$

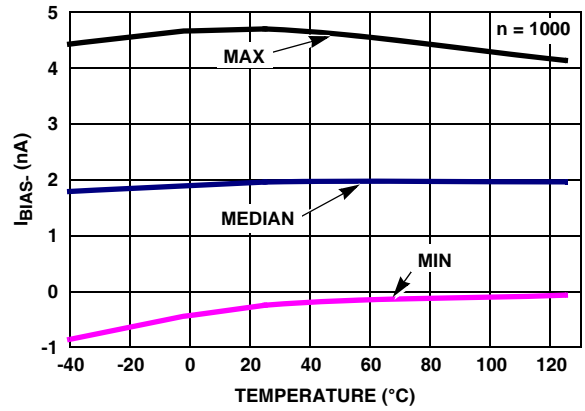


FIGURE 24.  $I_{BIAS-}$  vs TEMPERATURE  $V_S = \pm 2.5V$

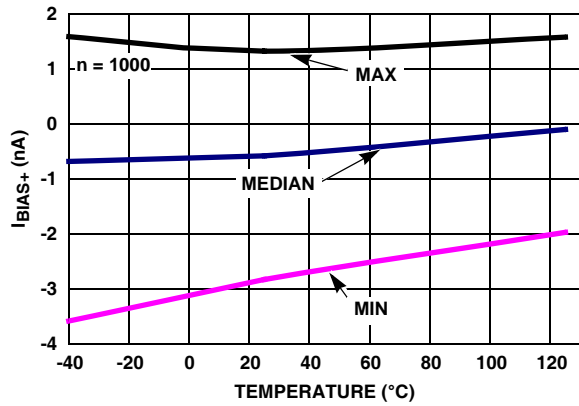


FIGURE 25.  $I_{BIAS+}$  vs TEMPERATURE  $V_S = \pm 1.5V$

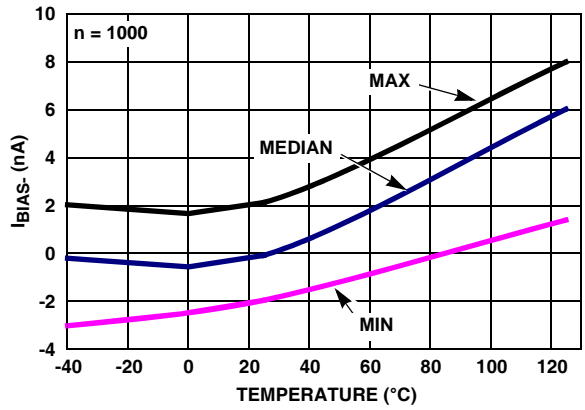


FIGURE 26.  $I_{BIAS-}$  vs TEMPERATURE  $V_S = \pm 1.5V$

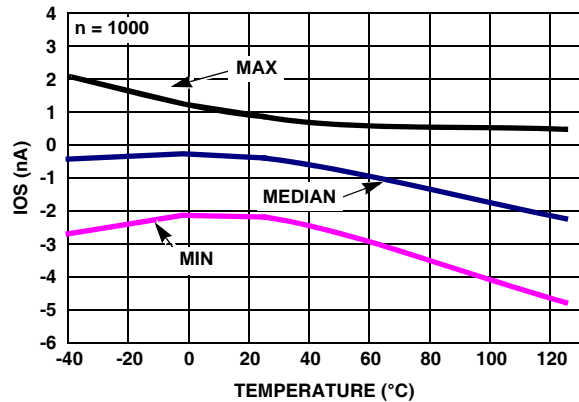


FIGURE 27. IOS vs TEMPERATURE  $V_S = \pm 2.5V$

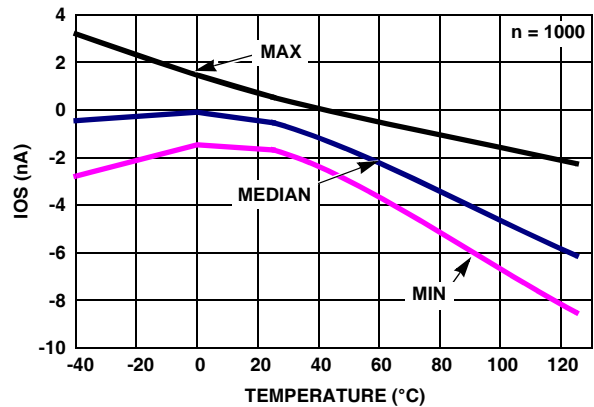


FIGURE 28. IOS vs TEMPERATURE  $V_S = \pm 1.5V$



Typical Performance Curves (Continued)

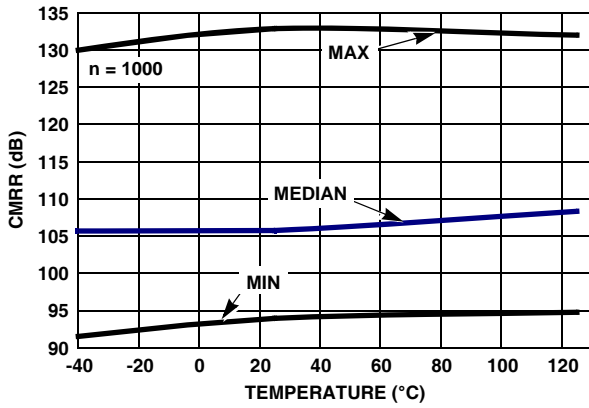


FIGURE 29. CMRR vs TEMPERATURE  $V_+ = \pm 2.5V, \pm 1.5V$

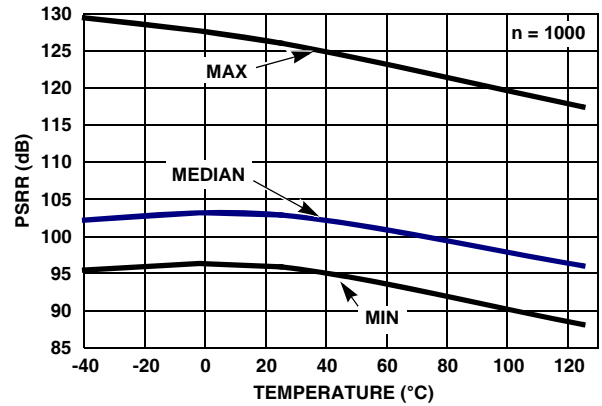


FIGURE 30. PSRR vs TEMPERATURE  $\pm 1.2V$  to  $\pm 2.5V$

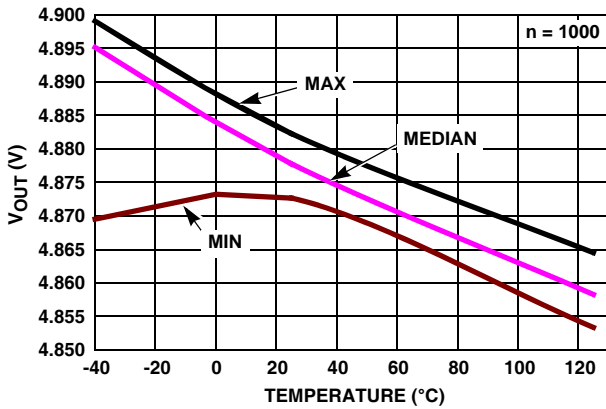


FIGURE 31.  $V_{OUT}$  HIGH vs TEMPERATURE  $V_S = \pm 2.5V, R_L = 1k$

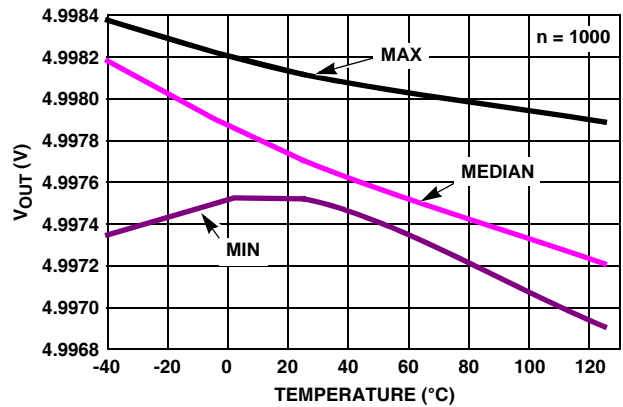


FIGURE 32.  $V_{OUT}$  HIGH  $V_S = \pm 2.5V, R_L = 100k$

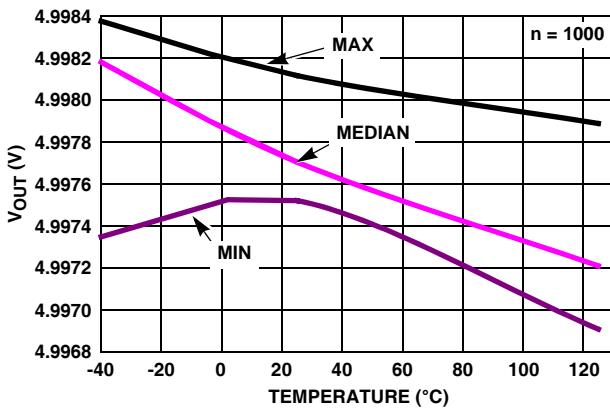


FIGURE 33.  $V_{OUT}$  LOW  $V_S = \pm 2.5V, R_L = 1k$

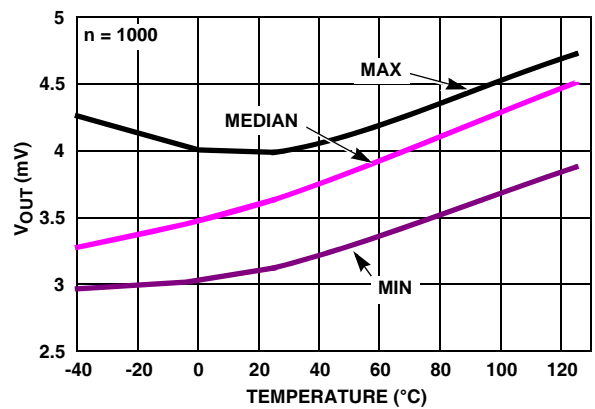
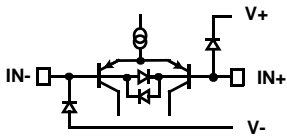
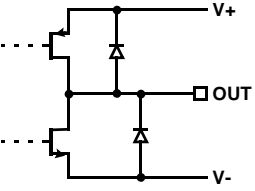
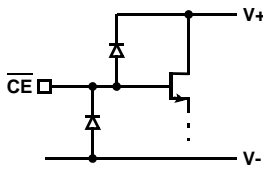


FIGURE 34.  $V_{OUT}$  LOW  $V_S = \pm 2.5V, R_L = 100k$

**Pin Descriptions**

ISL28156 (6 Ld SOT-23)	ISL28156 (8 Ld SO)	ISL28256 (8 Ld MSOP)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
	1, 5		NC	Not connected	
4	2	2 (A) 6 (B)	IN-	Inverting input	 <p>Circuit 1</p>
3	3	3 (A) 5 (B)	IN+	Non-inverting input	(See circuit 1)
2	4	4	V-	Negative supply	
1	6	1 (A) 7 (B)	OUT	Output	 <p>Circuit 2</p>
6	7	8	V+	Positive supply	
5	8		$\overline{\text{ENABLE}}$	Chip enable	 <p>Circuit 3</p>

**Applications Information**

**Introduction**

The ISL28156 is a single BiMOS rail-to-rail input, output (RRIO) operational amplifier with an enable feature. The ISL28256 is a dual version without the enable feature. Both devices are designed to operate from single supply (2.4V to 5.0V) or dual supplies ( $\pm 1.2V$  to  $\pm 2.5V$ ) while drawing only 39 $\mu A$  of supply current per amplifier. This combination of low power and precision performance makes this device suitable for a variety of low power applications including battery powered systems.

**Rail-to-Rail Input/Output**

These devices feature bipolar inputs which have an input common mode range that extends up to 0.5V beyond the v+ rail, and to within 10mV of the V- rail. The CMOS outputs typically swing to within about 4mV of the supply rails with a 100k $\Omega$  load. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction.

**Input Protection**

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to

within one diode beyond the supply rails. They also contain back-to-back diodes across the input terminals. For applications where the input differential voltage is expected to exceed 0.5V, external series resistors must be used to ensure the input currents never exceed 5mA (Figure 35).

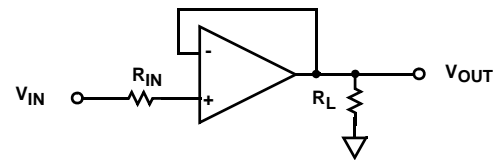


FIGURE 35. INPUT CURRENT LIMITING

**Enable/Disable Feature**

The ISL28156 offers an  $\overline{\text{EN}}$  pin that disables the device when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 10 $\mu A$ . By disabling the part, multiple ISL28156 parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the  $\overline{\text{EN}}$  pin. The  $\overline{\text{EN}}$  pin also has an internal pull down. If left open, the  $\overline{\text{EN}}$  pin will pull to the negative rail and the device will be enabled by default.

The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together.

**Using Only One Channel**

The ISL28256 is a dual op amp. If the application only requires one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 36).

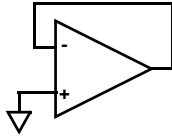


FIGURE 36. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

**Current Limiting**

These devices have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

**Power Dissipation**

It is possible to exceed the +125°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T<sub>JMAX</sub>) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} \times PD_{MAXTOTAL}) \tag{EQ. 1}$$

where:

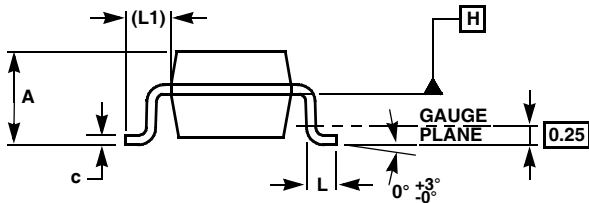
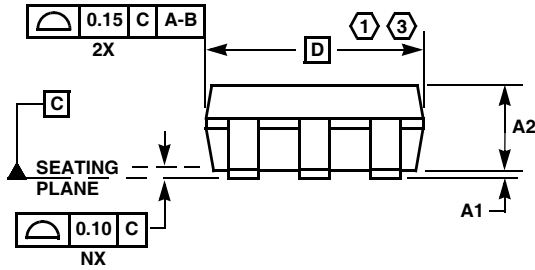
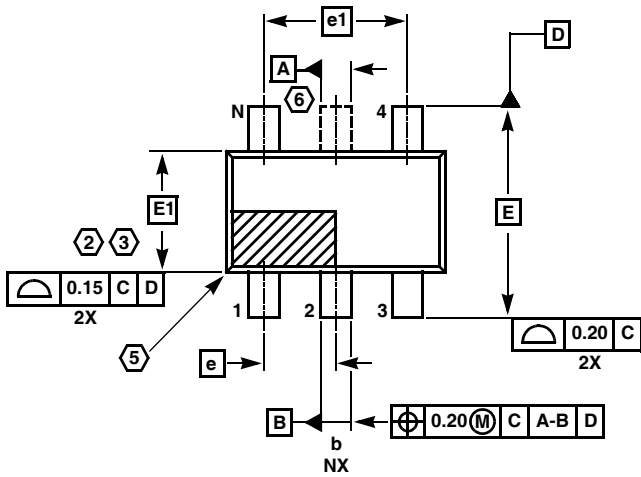
- PD<sub>MAXTOTAL</sub> is the sum of the maximum power dissipation of each amplifier in the package (PD<sub>MAX</sub>)
- PD<sub>MAX</sub> for each amplifier can be calculated as follows:

$$PD_{MAX} = 2 \times V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \tag{EQ. 2}$$

where:

- T<sub>MAX</sub> = Maximum ambient temperature
- θ<sub>JA</sub> = Thermal resistance of the package
- PD<sub>MAX</sub> = Maximum power dissipation of 1 amplifier
- V<sub>S</sub> = Supply voltage
- I<sub>MAX</sub> = Maximum supply current of 1 amplifier
- V<sub>OUTMAX</sub> = Maximum output voltage swing of the application
- R<sub>L</sub> = Load resistance

SOT-23 Package Family



MDP0038

SOT-23 PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

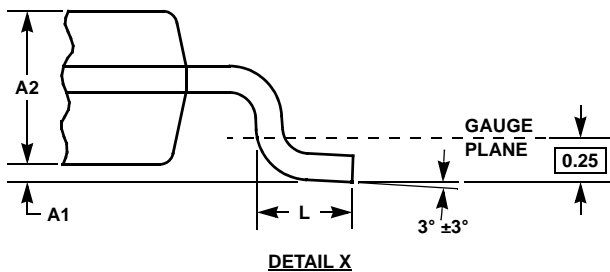
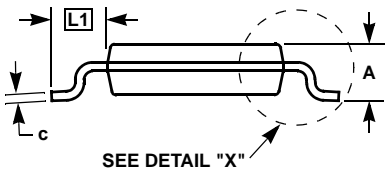
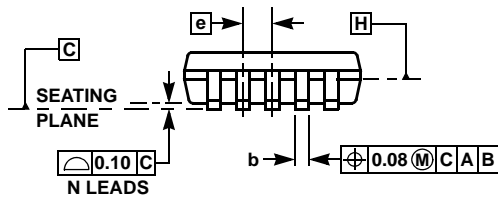
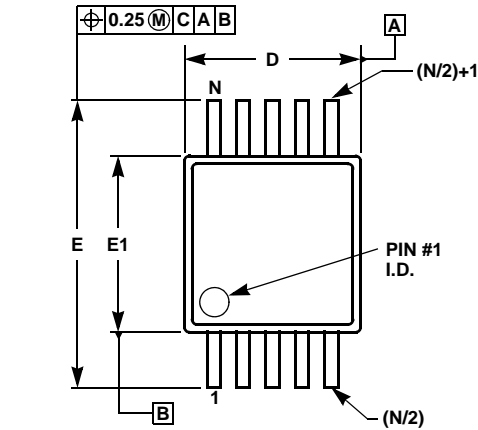
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	$\pm 0.003$	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	$\pm 0.002$	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	$\pm 0.003$	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	$\pm 0.001$	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	$\pm 0.004$	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	$\pm 0.008$	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	$\pm 0.004$	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	$\pm 0.009$	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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